POST-LAYOUT OPTIMIZATION IN INTEGRATED CIRCUIT DESIGN

ABSTRACT

A method for post-layout timing optimization is disclosed. The method performs timing analysis on a design to obtain timing information such as critical paths and slack values. Incremental placement based on the timing information is performed. A new routed design is generated by applying incremental routing to the result of incremental placement. The routed design is stored if its performance is better than the previous routed design. The above steps are repeated until a predetermined criterion is met.